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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,722	11/25/2003	Michael O'Connor	884.398US2	5763
21186	7590	07/01/2005	EXAMINER	
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. BOX 2938 MINNEAPOLIS, MN 55402-0938			TRINH, MICHAEL MANH	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/721,722

Applicant(s)

O'CONNOR ET AL.

Examiner

Michael Trinh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 11/25/2003.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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DETAILED ACTION

*** This office action is in response to filing of the application on November 25, 2003.

Claims 1-27 are pending.

Claim Objections

1. Claims 5,12,13,14 are objected to as indirect limitation and lacking antecedent basis for the term "processor" of the phrase "the semiconductor processor chip".
2. Claim 10 is objected to as "the heat conducting layer" lacking antecedent basis, although a diamond containing layer as disclosed is a heat conducting layer.

Correction is respectfully requested.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

- (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1-14,16-24,26-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Dahl et al (2002/0130407).

Dahl teaches a method of cooling a semiconductor chip, comprising: providing a number of electrical devices on a semiconductor layer of the semiconductor chip 601 (Figs 6A-6C and 9; paragraphs 0115-0121,0136-0141); integrally forming a substantially planar heat transfer conducting layer (620 in Figs 6B-6C, paragraphs 0120-0123; 910/911 in Fig 9; paragraphs 136-141), with the semiconductor layer of the semiconductor chip 601, wherein the heat conducting layer 620,910,911 is compatible with semiconductor processing techniques, the heat conducting layer being adjacent to the number of electrical devices, wherein the heat conducting layer of diamond is having a higher thermal conductivity than the semiconductor layer (paragraphs

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0120-0123;0131); conducting heat generated by the number of electrical devices into the heat conducting layer; and transmitting the heat generated by the number of electrical devices through the heat conducting layer 620,910,911 from a first region having a first temperature to a second region of a heat sink 610 (Figs 6B-6C; paragraphs 0120) having a second temperature that is lower than the first region. Re further claim 10, wherein the heating transfer conducting layer 620/910/911 comprises a diamond containing layer (paragraphs 0122;0138), wherein heat generated by the electrical devices are spreading in a first area through the heat transfer conducting layer to a larger second area wherein heat per unit area is reduced. Re further claims 16,21,26, wherein the method comprises fabricating a semiconductor layer; forming a number of electrical devices on the semiconductor layer; electrically connecting the number of electrical devices (Fig 9, paragraphs 0136-0141; and Figs 6A-6C, paragraphs 0115-0122), wherein the heat transfer conducting layer 620/910/911 comprises a diamond containing layer (paragraphs 0120-0122,0141), wherein, re further claim 26, the integrated circuit packaging includes the semiconductor chip coupling to memory, logic and microprocessing devices (paragraphs 0116) and wherein the memory includes a random access memory (paragraphs 0141). Re claim 2, wherein the electrical devices include a number of transistors (paragraphs 0115,0136-0137). Re claims 3,7,18, wherein the heat transfer conducting layer comprises a carbon-containing layer (paragraphs 0005-0020). Re claims 4,8,19, wherein the heat transfer conducting layer comprises a diamond containing layer (paragraphs 0120-0122; 0005-0020). Re claims 5,9,12, wherein heat is transmitted from the heat transfer conducting layer 620 to a location of heat sink 610 remote from the semiconductor chip (Fig 5B, paragraphs 0120). Re further claim 11, wherein the electrical devices include a number of transistors (paragraphs 0115,0136-0137). Re claim 14,24, wherein the diamond containing layer 620 (Fig 6B-6C; paragraphs 0120-0124) is formed on a back side of the semiconductor chip 601. Re claims 13,23, wherein the diamond containing layer 910/911 (Fig 9; paragraphs 0137-0138) is formed on an active side of the semiconductor chip. Re claim 17, wherein the semiconductor layer includes a silicon substrate (paragraphs 0136-0137;0115-0122). Re claim 20, wherein the diamond containing layer includes chemical vapor depositing a diamond layer (paragraphs 0122,0138,0103-0108). Re claims 22,27, wherein the electrical devices include a number of transistors on a silicon substrate (paragraphs 0115,0136-0137).

5. Claims 1-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Linn et al (5,569,620).

Linn teaches a method of cooling a semiconductor chip, comprising: providing a number of electrical devices on a semiconductor layer (e.g. 602; Fig 6) of the semiconductor chip; integrally forming a substantially planar heat transfer conducting layer 613/615 with the semiconductor layer (Fig 6; col 7, lines 35-56; Figs 3a-3g; col 3, line 30 through col 4), wherein the heat conducting layer 613/615 is compatible with semiconductor processing techniques, the heat conducting layer 613/615 being adjacent to the number of electrical devices, wherein the heat conducting layer (613 of diamond, 615 of silicide) is having a higher thermal conductivity than the semiconductor layer (col 7, lines 35-56); conducting heat generated by the number of electrical devices into the heat conducting layer; and transmitting the heat generated by the number of electrical devices through the heat conducting layer 613,615 from a first region having a first temperature to a second region 612 of having a second temperature that is lower than the first region. Re further claim 10, wherein the heating transfer conducting layer 613 comprises a diamond containing layer (col 7, lines 35-56), wherein heat generated by the electrical devices are spreading in a first area through the heat transfer conducting layer to a larger second area 612 wherein heat per unit area is reduced. Re further claims 16,21, wherein the method comprises fabricating a semiconductor layer; forming a number of electrical devices on the semiconductor layer; electrically connecting the number of electrical devices (Figs 6,1; col 7, lines 35-56; col 1, line 25 through col 2; Figs 3a-3g; col 3, line 30 through col 4), wherein the heat transfer conducting layer 613 comprises a diamond containing layer. Re claim 2, wherein the electrical devices include a number of transistors (col 1, line 25 through col 4; Fig 6, col 3, line 40 through col 4; Figs 3a-3g; col 3, line 30 through col 4). Re claims 3,7,18, wherein the heat transfer conducting layer comprises a carbon-containing layer (col 4, line 1). Re claims 4,8,19, wherein the heat transfer conducting layer comprises a diamond containing layer 613 (col 7, lines 35-56). Re claims 5,9,12, wherein heat is transmitted form the heat transfer conducting layer 613 to a location of 612 remote from the semiconductor chip (Fig 6). Re further claim 11, wherein the electrical devices include a number of transistors (col 1, line 25 through col 4; Fig 6, col 3, line 40 through col 4; Figs 3a-3g, col 3, line 30 through col 4).

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Re claim 14,24, wherein the diamond containing layer 613 is formed on a back side of the semiconductor layer 602 of the semiconductor chip. Re claims 15,25, wherein the diamond containing layer 613 is formed between an active side in the silicon 602 and a backside of the silicon 612 of the semiconductor processor chip. Re claim 17, wherein the semiconductor layer includes a silicon substrate (col 3, line 30 through col 4). Re claim 20, wherein the diamond containing layer includes chemical vapor depositing a diamond layer (col 3, lines 43-46). Re claim 22, wherein the electrical devices include a number of transistors on a silicon substrate (col 1, line 25 through col 4; Fig 6, col 3, line 40 through col 4; Figs 3a-3g, col 3, line 30 through col 4).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Linn et al (5,569,620), as applied to claims 1-25 above, taken with Bertin et al (6,255,899).

Linn teaches a method of cooling a semiconductor chip as applied to claims 1-5 and fully repeated herein, wherein the method comprises fabricating a semiconductor layer; forming a number of electrical devices on the semiconductor layer; electrically connecting the number of electrical devices (Figs 6,1; col 7, lines 35-56; col 1, line 25 through col 2; Figs 3a-3g; col 3, line

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30 through col 4), wherein the heat transfer conducting layer 613 comprises a diamond containing layer.

Linn lacks forming an electronic system by coupling the chip to a random access memory.

However, Bertin teaches forming an electronic system by coupling the semiconductor processor chip 112 to a random access memory (RAM) 114,116 (112 in Fig 1A; col 2, line 55 through col 3; chip 146 and RAM 148 in Figs 1C-1D; col 4, line 52 through col 5, lines 8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form an integrated circuit packaging of Linn by coupling the chip to a random access memory, as taught by Bertin. This is because of the desirability to form an electronic system such as a computer for processing software applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-16



Michael Trinh
Primary Examiner